



**V916865K28QB**  
**128M x 64 HIGH PERFORMANCE**  
**UNBUFFERED DDR2 SDRAM MODULE**

**Features**

- 240-pin, unbuffered dual in-line memory module
- JEDEC standard 1.8V ± 0.1V power supply
- VDDQ=1.8V ± 0.1V
- Fast data transfer rate: PC2-4200, PC2-5300, or PC2-6400
- Programmable CAS Latency(CL): 4, 5, 6
- Programmable Additive Latency(AL): 0, 1, 2, 3, 4 and 5
- Write Latency(WL)=Read Latency(RL)-1
- Programmable burst lengths: 4 or 8
- Differential data strobe (DQS, DQS#)  
(Single ended data strobe option)
- On-die termination (ODT)
- Adjustable data-output drive strength
- 64ms, 8192-cycle refresh
- Serial Presence Detect (SPD) with EEPROM

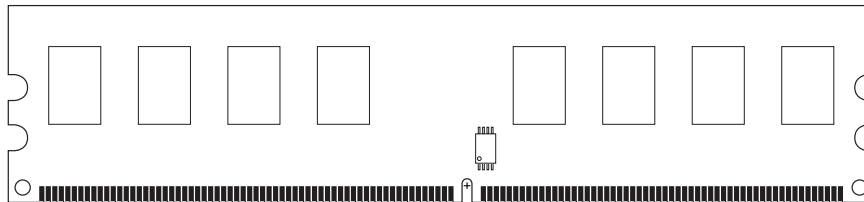
**Description**

The V916865K28QB memory module is organized as 134,217,728 x 64 bits in a 240 pin memory module. The 128M x 64 memory module uses 8 ProMOS 128M x 8 DDR2 SDRAMs. The x64 modules are ideal for use in high performance computer systems where increased memory density and fast access times are required.

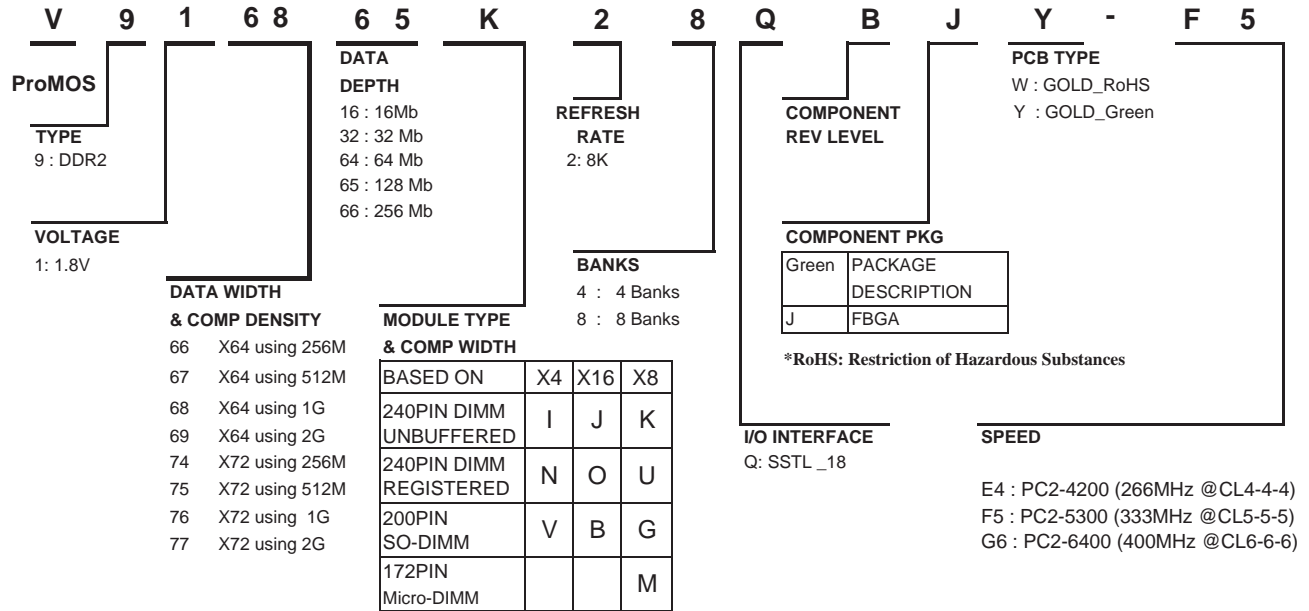
**Speed Grade**

	<b>DDR2-533 PC2-4200 (E4)</b>	<b>DDR2-667 PC2-5300 (F5)</b>	<b>DDR2-800 PC2-6400 (G6)</b>	<b>Units</b>
Bandwith@CL=4	533	533	533	Mbps
Bandwith@CL=5	533	667	667	Mbps
Bandwith@CL=6	533	667	800	Mbps
CL-tRCD-tRP	4-4-4	5-5-5	6-6-6	tCK

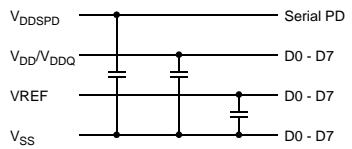
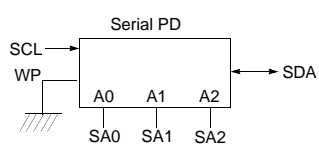
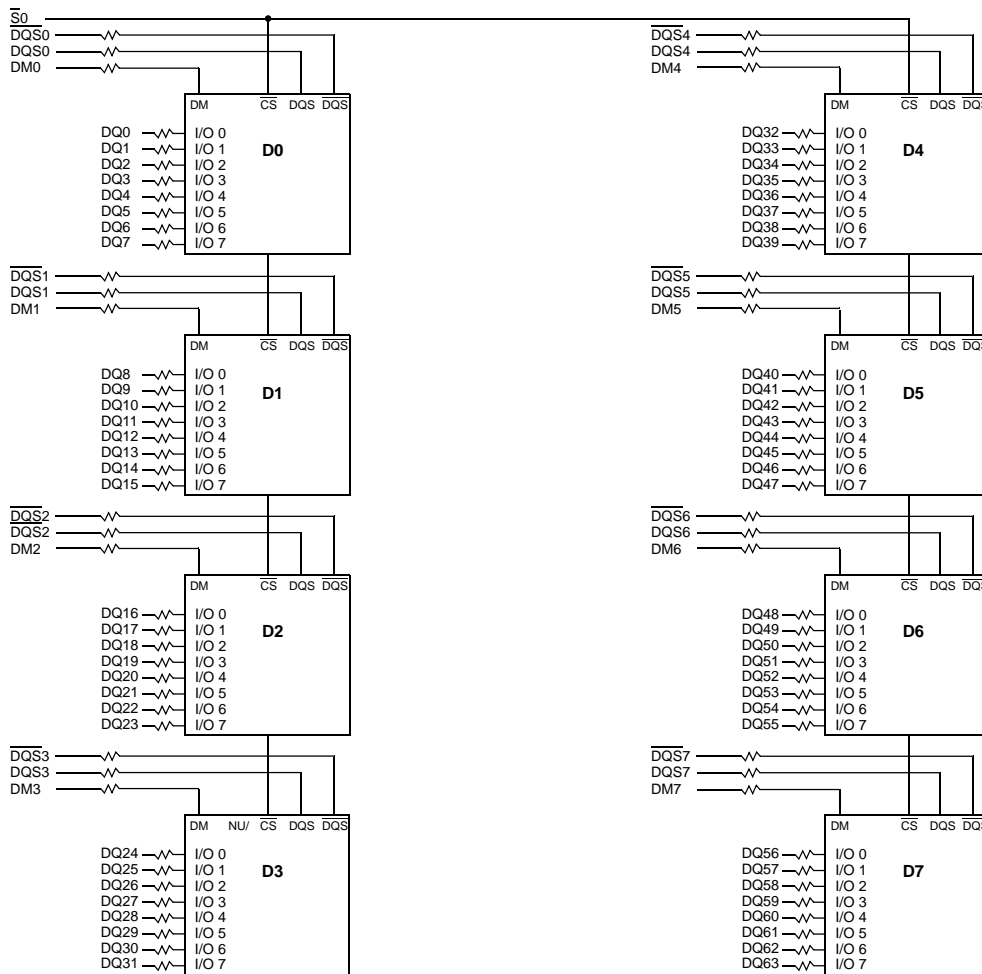
**240-pin DDR2 Unbuffered DIMM**



Part Number Information



Block Diagram



* Clock Wiring	
Clock Input	DDR2 SDRAMs
*CK0/CK0	2 DDR2 SDRAMs
*CK1/CK1	3 DDR2 SDRAMs
*CK2/CK2	3 DDR2 SDRAMs

- BA0 - BA1 → BA0-BA1 : DDR2 SDRAMs D0 - D7
- A0 - A13 → A0-A13 : DDR2 SDRAMs D0 - D7
- RAS → RAS : DDR2 SDRAMs D0 - D7
- CAS → CAS : DDR2 SDRAMs D0 - D7
- CKE0 → CKE : DDR2 SDRAMs D0 - D7
- WE → WE : DDR2 SDRAMs D0 - D7
- ODT0 → ODT : DDR2 SDRAMs D0 - D7

\*Wire per Clock Loading Table/Wiring Diagrams

- Notes :**
1. DQ,DM, DQS/DQS resistors : 22 Ohms 5%.
  2. BAx, Ax, RAS, CAS, WE resistors : 5.1 Ohms 5%.

**Pin Configuration (front/back side)**

**(240-pin DIMM Front)**

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	VREF	31	DQ19	61	A4	91	Vss
2	Vss	32	Vss	62	VDDQ	92	DQS5#
3	DQ0	33	DQ24	63	A2	93	DQS5
4	DQ1	34	DQ25	64	VDD	94	Vss
5	Vss	35	Vss	65	Vss	95	DQ42
6	DQS0#	36	DQS3#	66	Vss	96	DQ43
7	DQS0	37	DQS3	67	VDD	97	Vss
8	Vss	38	Vss	68	NC	98	DQ48
9	DQ2	39	DQ26	69	VDD	99	DQ49
10	DQ3	40	DQ27	70	A10/AP	100	Vss
11	Vss	41	Vss	71	BA0	101	SA2
12	DQ8	42	NC	72	VDDQ	102	NC
13	DQ9	43	NC	73	WE#	103	Vss
14	Vss	44	Vss	74	CAS#	104	DQS6#
15	DQS1#	45	NC	75	VDDQ	105	DQS6
16	DQS1	46	NC	76	NC	106	Vss
17	Vss	47	Vss	77	NC	107	DQ50
18	NC	48	NC	78	VDDQ	108	DQ51
19	NC	49	NC	79	Vss	109	Vss
20	Vss	50	Vss	80	DQ32	110	DQ56
21	DQ10	51	VDDQ	81	DQ33	111	DQ57
22	DQ11	52	CKE0	82	Vss	112	Vss
23	Vss	53	VDD	83	DQS4#	113	DQS7#
24	DQ16	54	NC	84	DQS4	114	DQS7
25	DQ17	55	NC	85	Vss	115	Vss
26	Vss	56	VDDQ	86	DQ34	116	DQ58
27	DQS2#	57	A11	87	DQ35	117	DQ59
28	DQS2	58	A7	88	Vss	118	Vss
29	Vss	59	VDD	89	DQ40	119	SDA
30	DQ18	60	A5	90	DQ41	120	SCL

**(240-pin DIMM Back)**

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
121	Vss	151	Vss	181	VDDQ	211	DM5
122	DQ4	152	DQ28	182	A3	212	NC
123	DQ5	153	DQ29	183	A1	213	Vss
124	Vss	154	Vss	184	VDD	214	DQ46
125	DM0	155	DM3	185	CK0	215	DQ47
126	NC	156	NC	186	CK0#	216	Vss
127	Vss	157	Vss	187	VDD	217	DQ52
128	DQ6	158	DQ30	188	A0	218	DQ53
129	DQ7	159	DQ31	189	VDD	219	Vss
130	Vss	160	Vss	190	BA1	220	CK2
131	DQ12	161	NC	191	VDDQ	221	CK2#
132	DQ13	162	NC	192	RAS#	222	Vss
133	Vss	163	Vss	193	S0#	223	DM6
134	DM1	164	NC	194	VDDQ	224	NC
135	NC	165	NC	195	ODT0	225	Vss
136	Vss	166	Vss	196	A13	226	DQ54
137	CK1	167	NC	197	VDD	227	DQ55
138	CK1#	168	NC	198	Vss	228	Vss
139	Vss	169	Vss	199	DQ36	229	DQ60
140	DQ14	170	VDDQ	200	DQ37	230	DQ61
141	DQ15	171	NC	201	Vss	231	Vss
142	Vss	172	VDD	202	DM4	232	DM7
143	DQ20	173	NC	203	NC	233	NC
144	DQ21	174	NC	204	Vss	234	Vss
145	Vss	175	VDDQ	205	DQ38	235	DQ62
146	DM2	176	A12	206	DQ39	236	DQ63
147	NC	177	A9	207	Vss	237	Vss
148	Vss	178	VDD	208	DQ44	238	VDDSPD
149	DQ22	179	A8	209	DQ45	239	SA0
150	DQ23	180	A6	210	Vss	240	SA1

**Pin Description**

Symbol	Type	Function
CK0-CK2 CK0#-CK2#	Input	CK and CK# are differential clock inputs. All the SDRAM addr/cntl inputs are sampled on the crossing of positive edge of CK and negative edge of CK#. Output (read) data is reference to the crossing of CK and CK# (Both directions of crossing)
CKE0-CKE1	Input	Activates the SDRAM CK signal when high and deactivates the CK Signal When low. By deactivating the clocks, CKE low initiates the Powe Down mode, or the Self-Refresh mode
S0#-S1#	Input	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disbled, new command are ignored but previous operations continue. This signal provides for external rank selection on systems with multiple ranks
RAS#, CAS#, WE#	Input	RAS#, CAS#, WE# (ALONG WITH CS#) define the command being entered.
ODT0-ODT1	Input	When high, termination resistance is enabled for all DQ, DQ# and DM pins, assuming the function is enabled in the Extended Mode Register Set (EMRS).
V <sub>REF</sub>	Supply	Reference voltage for SSTL 18 inputs.
V <sub>DDQ</sub>	Supply	Power supply for the DDR II SDRAM output buffers to provide improved noise immunity. For all current DDR2 unbuffered DIMM designs, VDDQ shares the same power plane as VDD pins.
BA0-BA1	Input	Selects which SDRAM BANK of four is activated.
A0-A13	Input	During a Bank Activate command cycle, Address input defines the row address (RA0-RA13)  During a Read or Write command cycle, Address input defines the colum address, In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If AP is low, autoprecharge is disbled. During a precharge command cycle, AP is used in conjunction with BA0, BA1 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0, BA1. If AP is low, BA0, BA1are used to define which bank to precharge.
DQ0-DQ63 CB0-CB7	In/Out	Data and Check Bit Input/Output pins.
DM0-DM8	Input	DM is an input mask signal for write data. Input data is masked when DM is sampled High coincident with that input data during a write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading.
V <sub>DD</sub> , V <sub>SS</sub>	Supply	Power and ground for DDR2 SDRAM input buffers, and core logic. VDD and VDDQ pins are tied to V <sub>DD</sub> /V <sub>DDQ</sub> planes on these modules.
DQS0-DQS8 DQS0#-DQS8#	In/Out	Data strobe for input and output data. its edge-aligned with read data, center aligned with write data. DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
SA0-SA2	Input	These signals and tied at the system planar to either V <sub>SS</sub> or V <sub>DD</sub> to configure the serial SPD EER-POM address range.
SDA	In/Out	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to VDD to act as a pullup on the system board.
SCL	Input	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to VDD to act as a pullup onthe system board.
V <sub>DD</sub> SPD	Supply	Power supply for SPD EEPROM. This supply is separate from the V <sub>DD</sub> /V <sub>DDQ</sub> power plane. EEPROM supply is operable from 1.7V to 3.6V.

**Serial Presence Detect Information**

Bin Sort:

E4 (PC2-4200 @ CL4)      F5 (PC2-5300 @ CL5)      G6 (PC2-6400 @ CL6)

Byte #	Function described	Function Supported			Hex value		
		E4	F5	G6	E4	F5	G6
0	Defines # of Bytes written into serial memory at module manufacturer	128bytes			80h		
1	Total # of Bytes of SPD memory device	256bytes			08h		
2	Fundamental memory type	SDRAM DDR2			08h		
3	# of row address on this assembly	14			0Eh		
4	# of column address on this assembly	10			0Ah		
5	Module attributes-Number of DIMM Ranks, Package and Height	1.18in., Single rank			60h		
6	Data width of this assembly	64 bits			40h		
7	.....Data width of this assembly	-			00h		
8	VDDQ and interface standard of this assembly	SSTL 1.8V			05h		
9	DDR SDRAM cycle time at CL=X	3.75ns	3.0ns	2.5ns	3Dh	30h	25h
10	DDR SDRAM Access time from clock at CL=X	±0.50ns	±0.45ns	±0.40ns	50h	45h	40h
11	DIMM configuration type(Non-parity, Parity, ECC)	Unbuffered			00h		
12	Refresh rate & type	7.8us & Self refresh			82h		
13	Primary DDR SDRAM width	x8			08h		
14	Error checking DDR SDRAM data width	N/A			00h		
15	Reserved	-			00h		
16	DDR SDRAM device attributes : Burst lengths supported	4,8			0Ch		
17	DDR SDRAM device attributes : # of banks on each DDR SDRAM	8 banks			08h		
18	DDR SDRAM device attributes : CAS Latency supported	4	4, 5	4,5,6	10h	30h	70h
19	DIMM Mechanical Thickness	<4.10mm			01h		
20	DDR2 DIMM Type	UDIMM			02h		
21	DDR2 SDRAM module attributes	-			00h		
22	DDR2 SDRAM device attributes : General	PASR/ODT 50ohm/Weak driver			07h		
23	DDR SDRAM cycle time at CL=X-1	-	3.75ns	3.0ns	00	3Dh	30h
24	DDR SDRAM Access time from CL=X-1	-	±0.50ns	±0.45ns	00	50h	45h
25	DDR SDRAM cycle time at CL=X-2	-		3.75ns	00		3Dh
26	DDR SDRAM Access time from CL=X-2	-		±0.50ns	00		50h
27	Minimum row precharge time (=t <sub>RP</sub> )	15ns	15ns	15ns	3Ch	3Ch	3Ch
28	Minimum row activate to row active delay (=t <sub>RRD</sub> )	7.5ns	7.5ns	7.5ns	1Eh	1Eh	1Eh
29	Minimum RAS to CAS delay (=t <sub>RCD</sub> )	15ns	15ns	15ns	3Ch	3Ch	3Ch
30	Minimum RAS pulse with t <sub>RAS</sub> (=t <sub>RAS</sub> )	45ns	45ns	45ns	2Dh	2Dh	2Dh
31	Module Rank density	1GB			01h		

Byte #	Function described	Function Supported			Hex value		
		E4	F5	G6	E4	F5	G6
32	Command and address signal input setup time	0.25ns	0.20ns	0.175ns	25h	20h	17h
33	Command and address signal input hold time	0.37ns	0.27ns	0.25ns	37h	27h	25h
34	Data signal input setup time	0.10ns	0.05ns	0.05ns	10h	05h	05h
35	Data signal input hold time	0.22ns	0.17ns	0.125ns	22h	17h	12h
36	Write Recovery Time (=t <sub>WR</sub> )	15ns			3Ch		
37	Write to Read CMD delay (=t <sub>WTR</sub> )	7.5ns	7.5ns	7.5ns	1Eh	1Eh	1Eh
38	Read to Precharge CMD delay (=t <sub>RTP</sub> )	7.5ns			1Eh		
39	Mem Analysis Probe	00	00	00	00		
40	Extension for bytes 41 and 42				06H		
41	SDRAM device minimum active to active/auto-refresh time (=t <sub>RC</sub> )	60ns	60ns	60ns	3Ch	3Ch	3Ch
42	SDRAM device minimum active to autorefresh to active/auto-refresh time (=t <sub>RFC</sub> )	127.5ns			7Fh		
43	SDRAM device maximum device cycle time (=t <sub>CK MAX</sub> )	8ns			80h		
44	SDRAM device maximum skew between DQS and DQ signals (=t <sub>DQSQ</sub> )	0.3ns	0.24ns	0.20ns	1Eh	18h	14h
45	SDRAM device maximum read datahold skew factor (=t <sub>QHS</sub> )	0.40ns	0.34ns	0.30ns	28h	22h	1Eh
46	PLL Relock Time	-			00h		
47	Tcase max , DT4R4W	00	00	00	00h	00h	00h
48	Thermal Resistance of DRAM Package from Top (Case) to Ambient	00	00	00	00h	00h	00h
49	DRAM case Temperature Rise from Ambient due to Active Pre-charge / Mode Bits (DT0/Mode Bits)	00	00	00	00h	00h	00h
50	DRAM case Temperature Rise from Ambient due to Precharge / Quiet Standby (DT2N/DT2O)	00	00	00	00h	00h	00h
51	DRAM case Temperature Rise from Ambient due to Precharge Power-Down (DT2P)	00	00	00	00h	00h	00h
52	DRAM case Temperature Rise from Ambient due to Active Standby (DT3N)	00	00	00	00h	00h	00h
53	DRAM case Temperature Rise from Ambient due to Active Power-Down with Fast PDN Exit (DT3Pfast)	00	00	00	00h	00h	00h
54	DRAM case Temperature Rise from Ambient due to Active Power-Down with Slow PDN Exit (DT3Pslow)	00	00	00	00h	00h	00h
55	DRAM case Temperature Rise from Ambient due to Page Open Burst Read / DT4R4W Mode bit (DT4R/DT4R4W)	00	00	00	00h	00h	00h
56	DRAM case Temperature Rise from Ambient due to Burst Refresh (DT5B)	00	00	00	00h	00h	00h
57	DRAM case Temperature Rise from Ambient due to Bank Inter-leave Reads with Auto-Precharge (DT7)	00	00	00	00h	00h	00h
58 - 61	Superset information (may be used in future)	-			00h		

Byte #	Function described	Function Supported			Hex value		
		E4	F5	G6	E4	F5	G6
62	SPD Revision	1.2			12h		
63	Checksum for Bytes 0 ~ 62	-			F5h	53h	E0h
64	Manufacturer JEDEC ID code	ProMOS			40h		
65 - 71	..... Manufacturer JEDEC ID code				00h		
72	Manufacturing location	02=Taiwan 05=China 0A=S-CH 04=Malaysia					
73 - 90	Module part number (ASCII)	V916865K28QB					
91	Manufacturer revision code (For PCB)	0			00		
92	Manufacturer revision code (For component)	0			00		
93	Manufacturing date (Year) in BCD. Example: Year 2006 = 06h	-			-		
94	Manufacturing date (Week) in BCD. Example: Week 28 = 28h	-			-		
95~98	Assembly serial #	-			-		
99~127	Manufacturer specific data (may be used in future)	Undefined			00h		
128~255	Open for customer use	Undefined			00h		

**Absolute Maximum DC Ratings**

Parameter	Symbol	MIN	MAX	UNITS
VDD Supply Voltage relative to VSS	VDD	-1.0	2.3	V
VDDQ Supply Voltage relative to VSS	VDDQ	-0.5	2.3	V
VDDL Supply Voltage relative to VSS	VDDL	-0.5	2.3	V
Voltage on any pin relative to VSS	VIN, VOUT	-0.5	2.3	V
Storage Temperature	T <sub>STG</sub>	-55	100	°C

Note: Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device.

**AC & DC Operating Conditions**  
**Recommended DC Operating Conditions**

Parameter	Symbol	MIN	NOM	MAX	UNITS	Notes
VDD Supply Voltage relative to VSS	VDD	1.7	1.8	1.9	V	1
VDDQ Supply Voltage relative to VSS	VDDQ	1.7	1.8	1.9	V	4
VDDL Supply Voltage relative to VSS	VDDL	1.7	1.8	1.9	V	4
I/O Reference Voltage	VREF	0.49xVDDQ	0.50xVDDQ	0.51xVDDQ	V	2
I/O Termination Voltage(system)	VTT	VREF-0.04	VREF	VREF+0.04	V	3

Note:

1. VDD and VDDQ must track each other. VDDQ must be less than or equal to VDD.
2. VREF is expected to equal to VDDQ/2 of the transmitting device and to track variations in the DC level of the same. Peak to Peak AC noise on the VREF may not exceed +/-2% VREF(DC).
3. VTT of the transmitting device must track VREF of receiving device.
4. VDDQ tracks with VDD; VDDL tracks with VDD.

**Input Electrical Characteristics and operating Conditions**

**Input DC Logic Levels**

Parameter	Symbol	MIN	MAX	UNITS
Input High (Logic 1) Voltage	VIH(DC)	VREF+0.125	VDDQ+0.3	V
Input Low (Logic 0) Voltage	VIL(DC)	-0.3	VREF-0.125	V

**Input AC Logic Levels**

Parameter	Symbol	DDR2 533		DDR2 667, 800		UNITS
		MIN	MAX	MIN	MAX	
ac input logic high	VIH(AC)	VREF+0.200	-	VREF+0.20	-	V
ac input logic low	VIL(AC)	-	VREF-0.200	-	VREF-0.200	V

DDR2 IDD Current Definitions

Symbol	Proposed Conditions	Units	Notes
IDD0	<b>Operating one bank active-precharge current;</b> t <sub>CK</sub> = t <sub>CK</sub> (IDD), t <sub>RC</sub> = t <sub>RC</sub> (IDD), t <sub>RAS</sub> = t <sub>RASmin</sub> (IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	mA	
IDD1	<b>Operating one bank active-read-precharge current;</b> I <sub>OUT</sub> = 0mA; BL = 4, CL = CL(IDD), AL = 0; t <sub>CK</sub> = t <sub>CK</sub> (IDD), t <sub>RC</sub> = t <sub>RC</sub> (IDD), t <sub>RAS</sub> = t <sub>RASmin</sub> (IDD), t <sub>RCD</sub> = t <sub>RCD</sub> (IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	mA	
IDD2P	<b>Precharge power-down current;</b> All banks idle; t <sub>CK</sub> = t <sub>CK</sub> (IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	mA	
IDD2Q	<b>Precharge quiet standby current;</b> All banks idle; t <sub>CK</sub> = t <sub>CK</sub> (IDD); CKE is HIGH, CS\ is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	mA	
IDD2N	<b>Precharge standby current;</b> All banks idle; t <sub>CK</sub> = t <sub>CK</sub> (IDD); CKE is HIGH, CS\ is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	mA	
IDD3P	<b>Active power-down current;</b> All banks open; t <sub>CK</sub> = t <sub>CK</sub> (IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0mA	mA
		Slow PDN Exit MRS(12) = 1mA	mA
IDD3N	<b>Active standby current;</b> All banks open; t <sub>CK</sub> = t <sub>CK</sub> (IDD), t <sub>RAS</sub> = t <sub>RASmax</sub> (IDD), t <sub>RP</sub> = t <sub>RP</sub> (IDD); CKE is HIGH, CS\ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	mA	
IDD4W	<b>Operating burst write current;</b> All banks open, Continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; t <sub>CK</sub> = t <sub>CK</sub> (IDD), t <sub>RAS</sub> = t <sub>RASmax</sub> (IDD), t <sub>RP</sub> = t <sub>RP</sub> (IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	mA	
IDD4R	<b>Operating burst read current;</b> All banks open, Continuous burst reads, I <sub>OUT</sub> = 0mA; BL = 4, CL = CL(IDD), AL = 0; t <sub>CK</sub> = t <sub>CK</sub> (IDD), t <sub>RAS</sub> = t <sub>RASmax</sub> (IDD), t <sub>RP</sub> = t <sub>RP</sub> (IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	mA	
IDD5B	<b>Burst auto refresh current;</b> t <sub>CK</sub> = t <sub>CK</sub> (IDD); Refresh command at every t <sub>RFC</sub> (IDD) interval; CKE is HIGH, CS\ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	mA	
IDD6	<b>Self refresh current;</b> CK and CK\ at 0V; CKE = 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	Normal	mA
		Low Power	mA
IDD7	<b>Operating bank interleave read current;</b> All bank interleaving reads, I <sub>OUT</sub> = 0mA; BL = 4, CL = CL(IDD), AL = t <sub>RCD</sub> (IDD) - 1 * t <sub>CK</sub> (IDD); t <sub>CK</sub> = t <sub>CK</sub> (IDD), t <sub>RC</sub> = t <sub>RC</sub> (IDD), t <sub>RRD</sub> = t <sub>RRD</sub> (IDD), t <sub>RCD</sub> = 1 * t <sub>CK</sub> (IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R; Refer to the following page for detailed timing conditions	mA	

**DDR2 IDD Current Table**

Symbol		E4 PC2-4200@CL4	F5 PC2-5300@CL5	G6 PC2-6400@CL6	Unit
IDD0		640	720	800	mA
IDD1		760	840	920	mA
IDD2P		120	120	120	mA
IDD2Q		320	360	400	mA
IDD2N		320	360	400	mA
IDD3P	Fast PDN Exit MR[12]=0	240	264	304	mA
	Slow PDN Exit MR[12]=1	144	144	144	mA
IDD3N		544	576	600	mA
IDD4R		2064	2256	2520	mA
IDD4W		2144	2336	2600	mA
IDD5B		2000	2080	2160	mA
IDD6		64	64	64	mA
IDD7		2160	2400	2480	mA

**AC Characteristics** (AC operating conditions unless otherwise noted)

Parameter	Symbol	(DDR2-533) -37		(DDR2-667) -3		(DDR2-800) -25		Unit	
		Min	Max	Min	Max	Min	Max		
Row Cycle Time	$t_{RC}$	60	-	60	-	57.5	-	ns	
Auto Refresh Row Cycle Time	$t_{RFC}$	127.5	-	127.5	-	127.5	-	ns	
Row Active Time	$t_{RAS}$	45	70K	45	70K	45	70K	ns	
Row Address to Column Address Delay	$t_{RCD}$	15	-	15	-	12.5	-	ns	
Row Active to Row Active Delay (x4 & x8)	$t_{RRD}$	7.5	-	7.5	-	7.5	-	ns	
Row Active to Row Active Delay (x16)	$t_{RRD}$	10	-	10	-	10	-	ns	
Column Address to Column Address Delay	$t_{CCD}$	2	-	2	-	2	-	CLK	
Row Precharge Time	$t_{RP}$	15	-	15	-	12.5	-	ns	
Write Recovery Time	$t_{WR}$	15	-	15	-	15	-	ns	
Last Data-In to Read Command	$t_{DRL}$	1	-	1	-	1	-	CLK	
Auto Precharge Write Recovery + Precharge Time	$t_{DAL}$	$t_{WR} + t_{RP}$	-	$t_{WR} + t_{RP}$	-	$t_{WR} + t_{RP}$	-	ns	
System Clock Cycle Time	$\overline{CAS}$ Latency = 3	$t_{CK}$	5	8	5	8	5	8	ns
	$\overline{CAS}$ Latency = 4		3.75	8	3.75	8	3.75	8	ns
	$\overline{CAS}$ Latency = 5		3.75	8	3	8	3	8	ns
	$\overline{CAS}$ Latency = 6		3.75	8	3	8	2.5	8	ns
Clock High Level Width	$t_{CH}$	0.45	0.55	0.48	0.52	0.48	0.52	CLK	
Clock Low Level Width	$t_{CL}$	0.45	0.55	0.48	0.52	0.48	0.52	CLK	
Data-Out edge to Clock edge Skew	$t_{AC}$	-0.50	0.50	-0.45	0.45	-0.40	0.40	ns	
DQS-Out edge to Clock edge Skew	$t_{DQSCK}$	-0.45	0.45	-0.40	0.40	-0.35	0.35	ns	
DQS-Out edge to Data-Out edge Skew	$t_{DQSQ}$	-	0.30	-	0.24	-	0.20	ns	
Data-Out hold time from DQS	$t_{QH}$	$t_{HPmin}$ $-t_{QHS}$	-	$t_{HPmin}$ $-t_{QHS}$	-	$t_{HPmin}$ $-t_{QHS}$	-	ns	
Data hold skew factor	$t_{QHS}$	-	400	-	340	-	300	ps	
Clock Half Period	$t_{HP}$	$t_{CH/L}$ min	-	$t_{CH/L}$ min	-	$t_{CH/L}$ min	-	ns	
Input Setup Time (fast slew rate)	$t_{IS}$	250	-	200	-	175	-	ps	
Input Hold Time (fast slew rate)	$t_{IH}$	375	-	275	-	250	-	ps	
Input Pulse Width	$t_{IPW}$	0.35	-	0.60	-	0.60	-	CLK	
Write DQS High Level Width	$t_{DQSH}$	0.35		0.35		0.35		CLK	
Write DQS Low Level Width	$t_{DQSL}$	0.35		0.35		0.35		CLK	
CLK to First Rising edge of DQS-In	$t_{DQSS}$	WL- $0.25t_{CK}$	WL+ $0.25t_{CK}$	WL- $0.25t_{CK}$	WL+ $0.25t_{CK}$	WL- $0.25t_{CK}$	WL+ $0.25t_{CK}$	CLK	
Data-In Setup Time to DQS-In (DQ & DM)	$t_{DS}$	100	-	100	-	50	-	ps	
Data-in Hold Time to DQS-In (DQ & DM)	$t_{DH}$	175	-	175	-	125	-	ps	

Parameter	Symbol	(DDR2-533) -37		(DDR2-667) -3		(DDR2-800) -25		Unit
		Min	Max	Min	Max	Min	Max	
DQS falling edge to CLK rising Setup Time	$t_{DSS}$	0.2	-	0.2	-	0.2	-	CLK
DQS falling edge from CLK rising Hold Time	$t_{DSH}$	0.2	-	0.2	-	0.2	-	CLK
DQ & DM Input Pulse Width	$t_{DIPW}$	0.35	-	0.35	-	0.35	-	CLK
Read DQS Preamble Time	$t_{RPRE}$	0.9	1.1	0.9	1.1	0.9	1.1	CLK
Read DQS Postamble Time	$t_{RPST}$	0.4	0.6	0.4	0.6	0.4	0.6	CLK
Write DQS Preamble Setup Time	$t_{WPRES}$	0	-	0	-	0	-	CLK
Write DQS Preamble Hold Time	$t_{WPREH}$	0.25	-	0.25	-	0.25	-	CLK
Write DQS Postamble Time	$t_{WPST}$	0.4	0.6	0.4	0.6	0.4	0.6	CLK
Internal read to precharge command delay	$t_{RTP}$	7.5	-	7.5	-	7.5	-	ns
Internal write to read command delay	$t_{WTR}$	7.5	-	7.5	-	7.5	-	ns
Data out high impedance time from CLK/ $\overline{\text{CLK}}$	$t_{HZ}$	$t_{AC(\text{min})}$	$t_{AC(\text{max})}$	$t_{AC(\text{min})}$	$t_{AC(\text{max})}$	$t_{AC(\text{min})}$	$t_{AC(\text{max})}$	ns
Data out low impedance time from CLK/ $\overline{\text{CLK}}$	$t_{LZ}$	$t_{AC(\text{min})}$	$t_{AC(\text{max})}$	$t_{AC(\text{min})}$	$t_{AC(\text{max})}$	$t_{AC(\text{min})}$	$t_{AC(\text{max})}$	ns
Mode Register Set Delay	$t_{MRD}$	2	-	2	-	2	-	CLK
Exit Self Refresh to Non-Read Command	$t_{XSNR}$	$t_{RFC}+10$	-	$t_{RFC}+10$	-	$t_{RFC}+10$	-	ns
Exit Self Refresh to Read Command	$t_{XSRD}$	200	-	200	-	200	-	CLK
Exit Precharge Power Down to any non-Read Command	$t_{XP}$	2	-	2	-	2	-	CLK
Exit Active Power Down to Read Command	$t_{XARD}$	2	-	2	-	2	-	CLK
Exit Active Power Down to Read Command (Slow exit, Lower Power)	$t_{XARDS}$	6-AL	-	7-AL	-	8-AL	-	CLK
ODT drive mode output delay	$t_{OIT}$	0	12	0	12	0	12	ns
Minimum time clocks remains ON after CKE asynchronously drops LOW	$t_{Delay}$	$t_{IS}+t_{CK}+t_{IH}$		$t_{IS}+t_{CK}+t_{IH}$		$t_{IS}+t_{CK}+t_{IH}$		ns
CKE minimum high and low pulse width	$t_{CKE}$	3	-	3	-	3	-	CLK

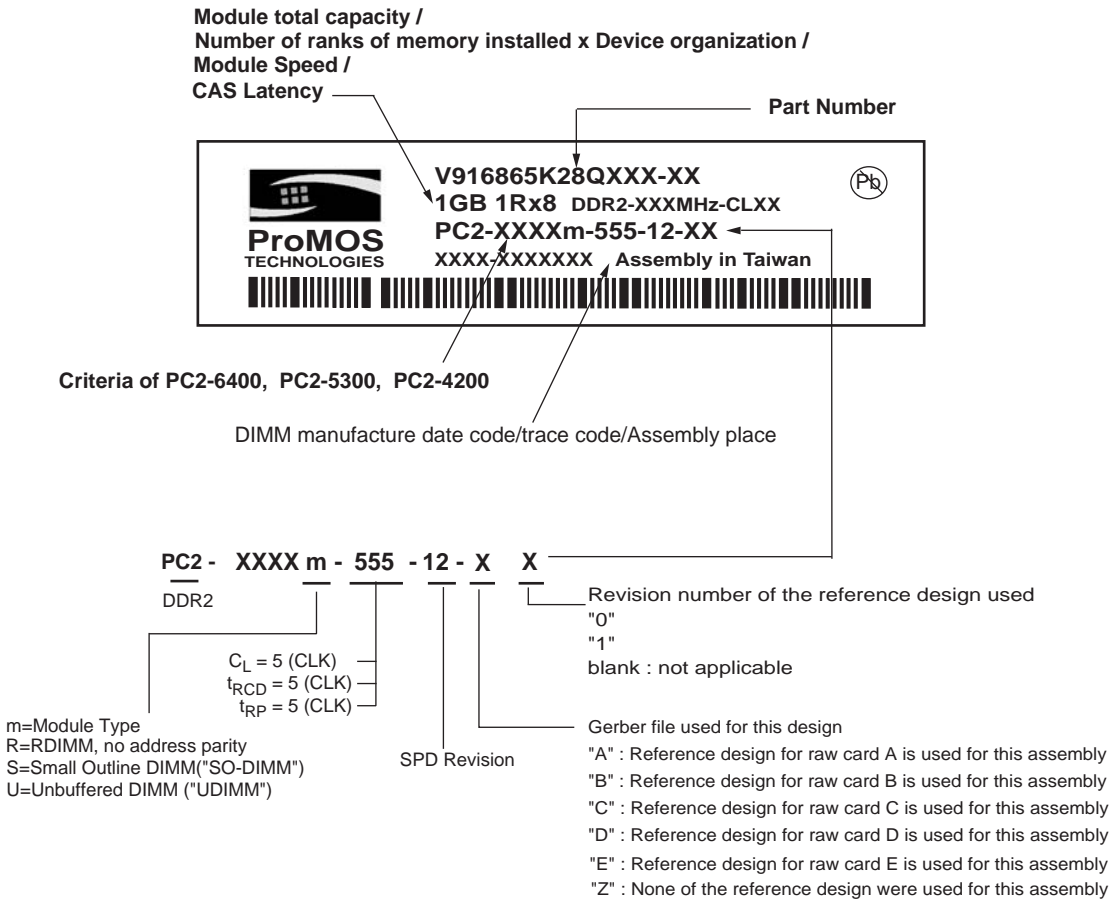
Package Dimension



NOTE:

All dimensions are in inches (millimeters);  $\frac{MAX}{MIN}$  or typical where noted.

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